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A 5-GHz Class-E Power Amplifier with an Inverse Class-B Driver on 65nm CMOS

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Abstract— The design and simulation of a Class-E power amplifier with an Inverse Class-B driver are presented. The Inverse Class-B amplifier generates a train of half sinusoids which provides a compromise between using a sine wave and a square wave as the input waveform. The design methodology proposed includes the use of load-pull technique to determine the optimum fundamental-frequency load-impedance of the amplifiers, and a series LC resonator to improve the second-harmonic suppression level. The PA exhibited 26.3 dB gain and 57% PAE at an output power of 21.3 dBm with the second and third harmonics attenuated to 38 and 37.3 dBc respectively.

Keywords—Cascode, Class-E, CMOS, driver, finite choke, high efficiency, integrated circuits, Inverse Class-B, planar inductors, power amplifier, second-harmonic trap, switched-mode.

I. INTRODUCTION

Upcoming wireless communication standards such as 5G are set to place greater demands on system complexity in order to meet consumer demand for higher data rates. This will require higher power consumption and thus will shorten battery lifetimes. As the power amplifier (PA) is responsible for the majority of the power consumption in a transceiver chain, it is of paramount importance to ensure that the PA's operation is highly efficient.

The switched-mode Class-E amplifier described in [1]–[3] offers a maximum DC-to-RF efficiency of 100% without the need for complex load networks seen in Class-F amplifiers. It integrates a shunt capacitor into its load network in order to increase the efficiency by reducing switching losses when the transistor is off by providing a path for the current.

Silicon CMOS process has made inroads at lower RF frequencies, e.g. 2.4 GHz and 5 GHz. Its low cost and high integration capability make it attractive despite poor performance due to the low resistivity substrate. The use of 65 nm CMOS allows the PA to be easily integrated with modern digital designs. Monolithic microwave integrated circuits (MMICs) at low RF frequencies require the use of lumped passive components as opposed to transmission lines since the implementation of the latter requires large chip areas. Poor unloaded quality-factor (Q) of planar inductors due to the lossy substrate and thin metallization layers increase the difficulty of realizing high efficiency designs. Further, the low oxide breakdown voltages in silicon present an issue due to the high peak voltages seen in the Class-E PA. This stress can be reduced with a cascode design.

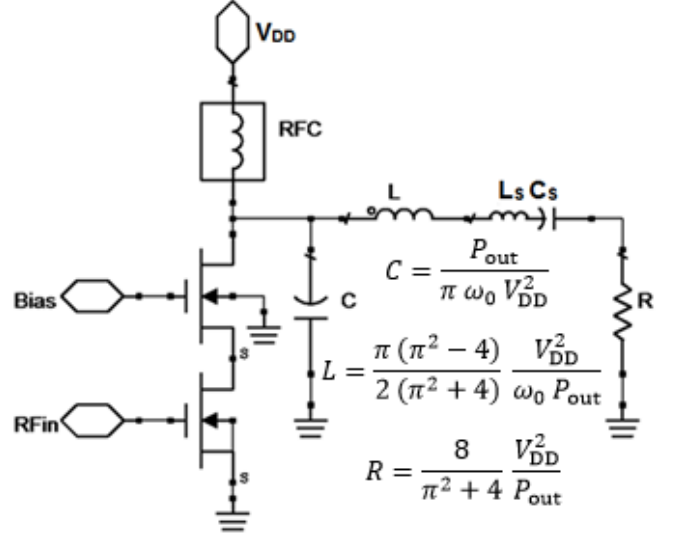


Fig. 1. An idealized cascode Class-E power amplifier.

In this paper, the design of a cascode Class-E PA cascaded with an Inverse Class-B driver on 65 nm CMOS will be described. The use of mixed voltage transistors can enable higher efficiency with a fast low-voltage transistor being protected by a higher voltage transistor. Load-pull technique is used to determine the optimum fundamental-frequency load-impedance of the PA (Z_{OPT}) to give best trade-off between output power and PAE whereas the PA's load impedances at harmonic frequencies are set to a high value, i.e. similar to the Class-E mode. A simple output matching circuit is employed to transform 50 Ω load resistance to Z_{OPT} . To further suppress the unwanted second-harmonic signal, the shunt capacitance in the matching circuit is replaced with a series LC tank tuned to $2f_0$. The added benefit of applying this strategy is that the PA's output power and efficiency are also improved.

II. CASCODE CLASS-E POWER AMPLIFIER AND INVERSE CLASS-B DRIVER TOPOLOGIES

An idealized cascode Class-E amplifier is shown in Fig. 1. It is comprised of transistors with an output network of a shunt capacitor C , a series inductor L , a series $L_s C_s$ resonator tuned to the fundamental frequency, and a load resistance R . The capacitor C_s also acts as a DC-blocking capacitance. Here, the

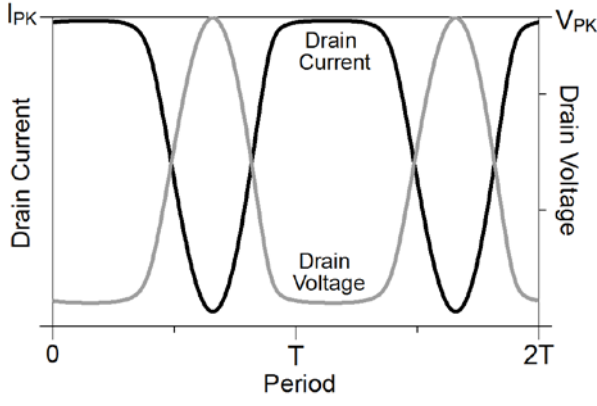


Fig. 2. Drain current and voltage waveforms of an Inverse Class-B amplifier.

transistor is driven sufficiently hard to behave as a switch in order to minimize the current/voltage overlap (power dissipation) across the device and thus improve the efficiency. The inductor L is used to provide a phase shift in order to ensure that the switch is fully off and that the capacitor C has discharged before the switch is turned on again. The $L_S C_S$ filter is used to remove the harmonic components generated by the transistor and the use of a square driving wave. The Class-E topology has a theoretical peak switch voltage of $3.56 \times V_{DD}$ which increases the risk of oxide breakdown in silicon devices. This can be alleviated with the use of the cascode/stacked topology to spread the voltage over multiple devices.

The Inverse Class-B amplifier is described in [4] as a method of shaping the drain voltage in order to drive another stage. The transistor is biased at V_{DD} and the negative swing of the input will generate a train of half sine-wave voltage pulses as seen in Fig. 2. This provides a compromise between driving the amplifier with a sine wave and a square wave. Compared to the Class-B amplifier, this topology has a lower theoretical maximum efficiency of 57.6% as shown in [4].

III. AMPLIFIER DESIGN METHODOLOGY

The amplifier was designed to operate at a centre frequency of 5 GHz, and in particular meet the following specifications: (i) output power (P_{out}) > 20 dBm, (ii) gain > 20 dB, (iii) drain efficiency and power added efficiency (PAE) > 50%, and (iv) 2nd and 3rd harmonic suppression levels > 30 dBc. Keysight's Advanced Design System (ADS) was used to design, simulate, and optimize the circuit. The full schematic is shown in Fig. 3 with the component values given in Table I.

The Inverse Class-B driver used a 1 V 65nm transistor with a total gate width of 576 μm . The supply voltage (V_{DD1}) was set to 0.4 V to limit the peak output voltage to below 1 V whereas V_{GG1} was also set to 0.4 V. A load-pull test for the driver was performed using an actual inductor model L_2 (provided by the foundry and confirmed through Momentum simulation) to provide a DC path for the drain biasing. No DC blocking capacitance was needed at the driver's output since the driver's DC supply voltage (i.e. V_{DD1}) was also used to provide a suitable gate biasing voltage for the PA stage. The test was repeated with various inductance values to find the optimal efficiency and output waveform. The driver was then sized such that its output

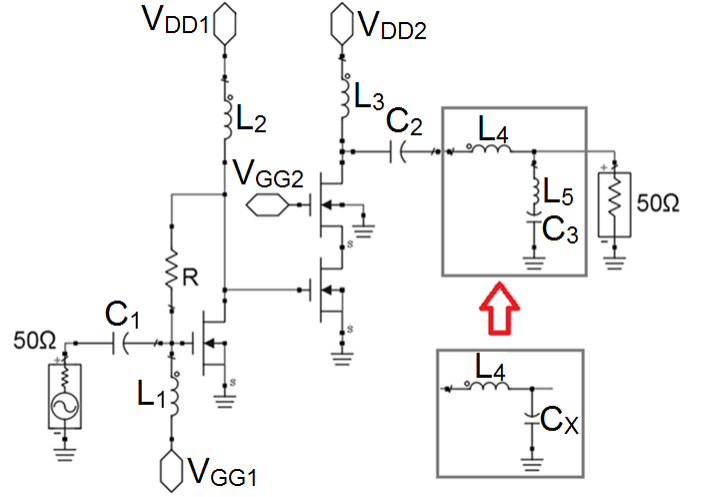


Fig. 3. Schematic of the complete amplifier circuit.

TABLE I. CIRCUIT COMPONENT VALUES

$L_1 = 0.87 \text{ nH } (Q = 20.0)$	$C_1 = 0.55 \text{ pF}$
$L_2 = 0.50 \text{ nH } (Q = 22.0)$	$C_2 = 5.19 \text{ pF}$
$L_3 = 0.75 \text{ nH } (Q = 21.4)$	$C_3 = 0.42 \text{ pF}$
$L_4 = 1.28 \text{ nH } (Q = 16.6)$	$C_X = 0.56 \text{ pF}$
$L_5 = 0.62 \text{ nH } (Q = 22.1)$	$R = 500 \text{ } \Omega$

impedance would be similar to the input impedance of the PA stage. This dispenses the need for an inter-stage matching circuit at the expense of a minor performance penalty.

The output stage used a 1V 65nm transistor with a width of 1344 μm connected by its drain to a 2.5V 280nm transistor with a width of 2016 μm . Here, V_{GG2} and V_{DD2} are set to 1.7 V and 2.5 V, respectively. A load pull simulation was performed to determine the optimum fundamental-frequency load impedance of the PA to give best trade-off between output power and PAE. Here the PA's load impedances at harmonic frequencies are set to a high value, i.e. similar to the Class-E mode. The values of DC feed inductance L_3 and DC blocking capacitance C_2 were fixed during the load pull simulations. This procedure was repeated for different sets of L_3 - C_2 values until an optimum point was obtained.

A simple L-type output-matching network (L_4 - C_X) was employed to present the optimal impedance of $19.5 + j18.1 \text{ } \Omega$ to the transistor and, owing to its low-pass-filter characteristic, to attenuate unwanted harmonic components. The Smith chart utility in ADS allows the unloaded Q for each passive element to be set to aid in accurate matching. However, the loaded Q of the filter is often not high enough so other more sophisticated (higher order) filter configurations need to be used instead to ensure proper harmonics terminations. But this translates into higher component count. To improve the 2nd harmonic attenuation while keeping the component count to a minimum, the shunt capacitance C_X in the matching network was replaced with a series L_5 - C_3 resonator tuned at $2f_0$ in order to provide a short-circuit to ground for the second harmonic signal, (1). The resonator needs to be sized in such a way that it presents the original value of C_X at f_0 , (2). At $3f_0$, this resonator will behave

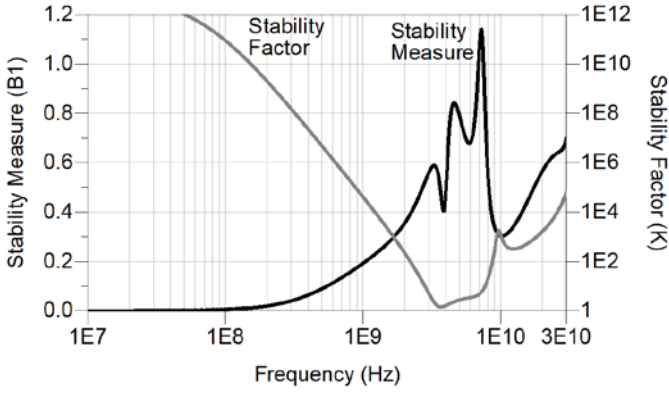


Fig. 4. Stability factor (k) and stability measure ($B1$).

like an inductor which will reduce the attenuation of the third harmonic component. The components values were then tuned to maximize the circuit efficiency.

$$L_5 = \frac{1}{4 \omega_0^2 C_3} \quad (1)$$

$$C_3 = \frac{3}{4} C_X \quad (2)$$

A high-pass filter network was used for the input match. The shunt inductor and series capacitor also fulfill the role of providing a DC path for the gate biasing and preventing the DC signal from flowing into the input port, respectively. A 500 Ω feedback resistor was employed to ensure unconditional stability, resulting in stability factor (k) > 1 and stability measure ($B1$) > 0 between 10 MHz - 30 GHz as shown in Fig. 4.

IV. SIMULATION RESULTS

Fig. 5 shows the PA performance against the input power where the output power and PAE of the proposed PA at -5 dBm input power are 21.3 dBm and 57%, respectively. The -3 dB bandwidth of the amplifier is 3.38 GHz with the PAE dropping to 27.3% at 3.21 GHz and 34.3% at 6.59 GHz. The PA performance is summarized and compared with other similar works in Table II.

V. CONCLUSION

The design, simulation, and optimization of a 65 nm cascode Class-E power amplifier with an Inverse Class-B driver have been demonstrated with the PA achieving a gain of 26.3 dB and a PAE of 57% at an output power of 21.3 dBm.

ACKNOWLEDGMENTS

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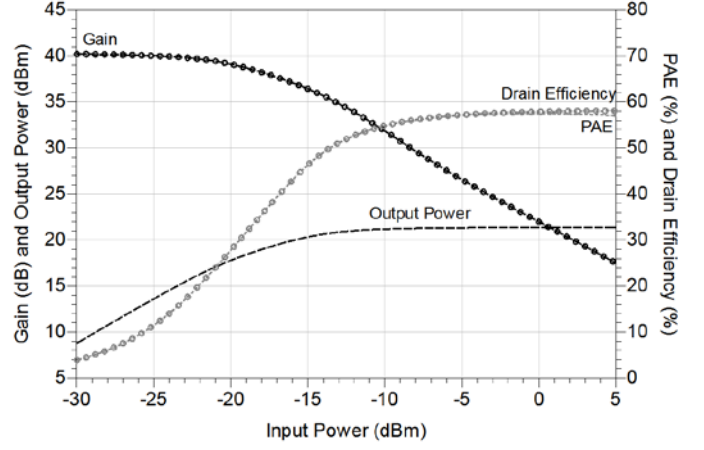


Fig. 5. Gain, output power, PAE and drain efficiency versus input power.

TABLE II. PERFORMANCE COMPARISONS

Parameter	This work*	[5]	[6]*	[7]	[8]	[9]*
Frequency (GHz)	5	5	5	2.5	2.4	2.2
Process (nm)	65	180	65	130	180	130
Supply (V)	2.5	2.3	1.36	2	2.4	3.3
Gain (dB)	26.3	21	9.3	31	31	N/A
Pout (dBm)	21.3	16.4	22.1	19	23	28.5
PAE (%)	57	35.4	40	32	42	47
Attenuation at $2f_0$ and $3f_0$ (dBc)	38/37.3	N/A	N/A	42/33	N/A	N/A

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